MOTOROLA
Semiconductor Products Inc.

AN-828
Application Note

THE EFFECTS OF BASE DRIVE CONDITIONS ON RBSOA

This application note describes the turn-off stresses placed on high voltage power transistors when used in clamped inductive load switching applications. The effects of off-bias voltage $V_{BE(off)}$, reverse base current I_{B2}, forward base current I_{B1} and temperature on the RBSOA capability and switching speeds are illustrated. Also described is the non-destruct RBSOA test circuit used in generating this data.

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INTRODUCTION

The reduction of inductive turn-off switching losses for high voltage power switching transistors is of prime importance in switching applications. This is generally accomplished by reverse biasing the base-emitter junction during turn-off time, thus quickly "sweeping out", or depleting the stored charge in the base-collector region of the transistor. This biasing can be derived by applying a reverse or off-bias voltage to the base through a low impedance source, resulting in a negative (reverse) base current I_{B2} flowing or through a constant current source.

As a result of the reverse bias, the storage time t_{sv}, the current fall time t_{fi} and the cross-over time t_c (a measure of the switching losses) can be substantially reduced. Also, as a consequence of this reverse bias and faster switching, the Reverse Bias Safe Operating Area (RBSOA) capability can be increased for certain types of high voltage power switching transistors. Characterization of these transistors (triple diffused and double diffused epitaxial collector) has shown operation in the turn-off clamped inductive mode to the V_{CEV} (the collector-emitter voltage with the base reversed bias) rating of the device, a voltage generally a couple of hundred volts greater than the V_{CEO} rating.

The V_{CEO} voltage is of importance when operating the transistor during turn-on and is a limitation on the familiar forward bias, or active region SOA curve. However, during inductive turn-off this curve is not applicable as there are different energy stresses placed on the device, ie: during turn-on, the emitter current is concentrated at the periphery of the emitter finger whereas, during turn-off, the current is crowded in the center of the emitter.

$E_{s/b}$

Power transistors were originally characterized with an unclamped inductive load as shown in Figure 1(A). The Transistor Under Test (T.U.T.), typically a low voltage, extremely rugged transistor, is turned on by applying a positive pulse to its base through a resistive network terminated in a reverse bias voltage V_{BB2}. Collector current then ramps up at a rate dictated by the time constant of the relatively large inductance in the collector circuit. When the T.U.T. turns off, the energy stored in the inductor ($E = \frac{1}{2} LI_{CM}^2$) has to be dissipated in the transistor since there is no external circuit, or clamp to "catch" this energy and the current ramps down. Also, immediately at turn-off, the collector-emitter voltage flies back up due to the "inductive kick" ($V = L\ di/dt$). If the energy stored is great enough and the transistor turn-off time fast enough, this voltage will flyback to the breakdown voltage of the device $V_{(BR)CEX}$, avalanching the collector of the transistor. The transistor thus has to dissipate the energy due to this unclamped operation — breakdown voltage and ramp down collector current for the time required to discharge the inductor. The maximum energy that the device can sustain, defined as Reverse Bias Secondary Breakdown Energy ($E_{s/b}$), is determined by increasing I_C until the device fails; usually this current is below the nominal operating current of the device. Theory and practice have shown that most low voltage transistors have decreasing $E_{s/b}$ capability with increasing reverse bias voltage due to current crowding.

The problem with this $E_{s/b}$ rating is that the derived energy is only related to that particular inductance and is also highly dependent on its Q (quality factor — ie: series resistance). Second, the inductance specified to

achieve $E_{s/b}$ is generally quite large, 10 mH or greater, and does not represent the real world inductance seen in switchmode applications. Third, and most important, most applications use some form of clamping to prevent collector voltage breakdowns.

RBSOA

Recognizing the need for a more precise and definitive inductive turn-off rating, Motorola initiated during the mid-70's a clamped inductive turn-off rating and labeled it RBSOA. Using the simplified test circuit of Figure 1(B), the T.U.T. is now subjected to a real world clamped condition. The inductance now used only need be large enough to ensure that the flyback time is greater than the collector current falltime, generally resulting in inductances of from 100 μH to 1.0 mH. These values also more accurately represent the leakage inductances encountered in switching applications. To subject the device to the greatest stress during turn-off, the inductance should be of high Q to ensure that the collector peak current I_{CM} and flyback voltage V_{CEM} are nearly simultaneously presented to the T.U.T., Figure 1(C), resulting in a turn-off load line that approximates a rectangle. Under these conditions, I_c will start to fall when V_{CE} forward bias the clamp diode, at which time the stored inductor energy (current) will be transferred to the external diode circuit.

To determine the RBSOA capability of the device, the peak collector current I_{CM} is set to a typical operating current (including $I_{C(max)}$) and the clamp voltage increased until the transistor generally goes into second breakdown. This second breakdown point relates to the energy dissipated in the transistor during turn-off, specifically t_c, and represents the energy encountered in inductive switching applications, (whereas, the lower I_{CM} for the unclamped $E_{s/b}$ mode does not). Reverse biasing in this example is provided by a transistor clamp from the base of the T.U.T. to a negative voltage source $-V_{BE(off)}$. In reality, the T.U.T. base voltage during turn-off, after the stored charge is removed, will be about 0.1 V higher due to $V_{CE(sat)}$ of the clamp transistor. For measurement simplicity, the power supply for generating the reverse bias voltage will be used throughout this article and will be defined as $V_{BE(off)}$.

THE EFFECTS OF REVERSE BIASING TURN-OFF

Base drive timing is as shown in Figure 1(B); I_{B1} is applied for some pulse duration and $V_{BE(off)}$ is then initiated concurrent with the fall time of I_{B1}. The intent of reverse biasing the base of the Switchmode Transistor* is to reduce t_{off} and thus minimize this switching loss. This is shown in Figure 2 where the inductive load turn-off times t_{sv}, t_{fi}, and t_c of a typical 2N6545 are shown plotted as a function of $V_{BE(off)}$; (t_{sv} is the inductive load storage time as measured from the 90% point on the I_{B1},I_{B2} transition to the 10% point of the V_{CE} voltage rise-time; t_{fi} is the inductive collector current fall-time between the 90% and 10% points).

As would be expected, t_{sv} is greatly reduced with

FIGURE 1, Inductive Load Switching

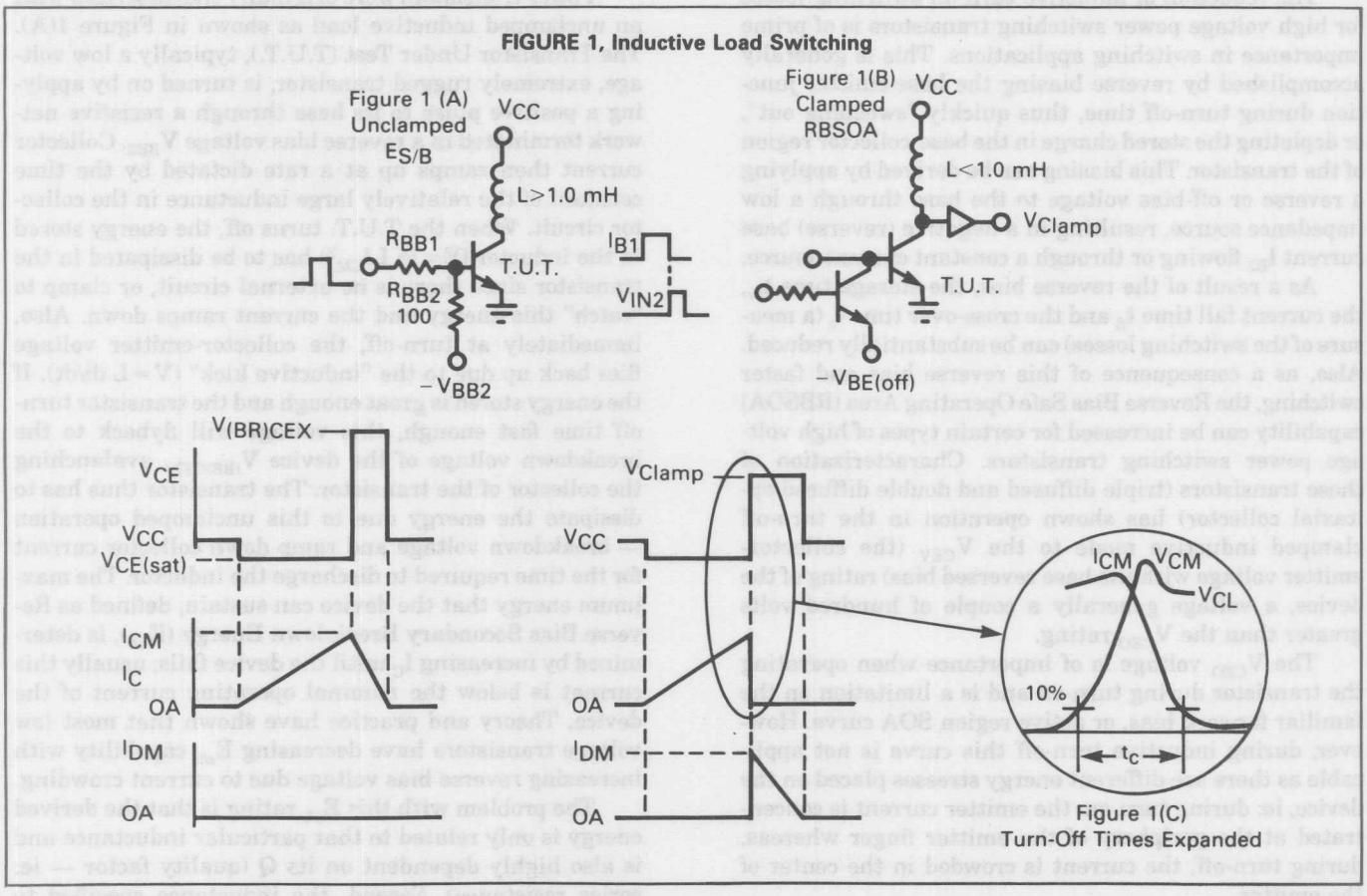


Figure 1(C)
Turn-Off Times Expanded

increasing $V_{BE(off)}$, varying from about 15 μs with zero bias to about 1.5 μs with −5.0 V bias; increasing the bias to as high as −11 V resulted in a further reduction of t_{sv} to about 0.8 μs. Similarly, t_{fi} was reduced from about 1.4 μs to 0.20 μs for 0 V and −5.0 V respectively, with the fall time then increasing to about 0.23 μs at −11 V. The crossover time t_c also decreased with increasing off-bias. Note that the maximum reverse bias of −11 V exceeded the specified V_{EBO} of −9.0 V. Although the device was operated in the emitter-base avalanche mode, no degradation occurred other than a reduction in low current beta.[3]

FIGURE 2, TYPICAL CLAMPED INDUCTIVE TURN-OFF SWITCHING TIMES FOR THE 2N6545 VERSUS $V_{BE(off)}$

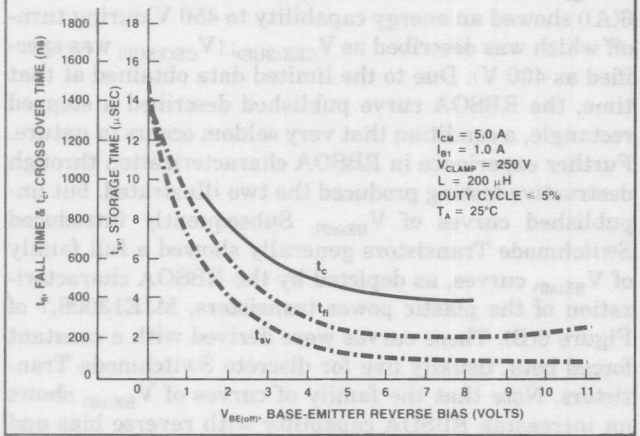


FIGURE 3, TYPICAL TURN-OFF TIMES FOR A RESISTIVE AND CLAMPED INDUCTIVE LOADS AS A FUNCTION OF REVERSE BASE CURRENT I_{B2}

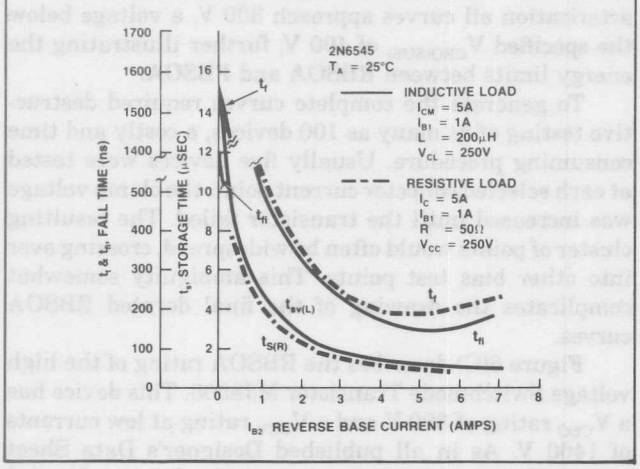


Figure 3 describes the turn-off times of the same 2N6545 as a function of I_{B2} for both a 5.0 A resistive load and a 5.0 A peak inductive load. To generate this data, the reverse bias clamp transistor was reconfigured as a constant current source with the driving voltage approaching −20 V for the 7.0 A I_{B2} condition. As in the previous illustration, turn-off times decreased with increasing I_{B2}, but t_{fi} and t_f again started to increase when I_{B2} exceeded about 5.0 A.

A further comparison between $V_{BE(off)}$ and I_{B2} is shown in the 2N6547 inductive turn-off photographs of Figures 4(A) and (B). Figure 4(A) illustrates the voltage source case where $V_{BE(off)}$ equals −3.0 V resulting in a I_{B2} of 3.0 A peak (I_{CM} = 4.0 A). Figure 4 (B) shows the current source case where I_{B2} is set equal to the 3.0 A voltage source example by adjusting the driving voltage to about −11 V. The storage time is the same for both cases, but the current source t_{fi} and t_c is lower than the voltage source.

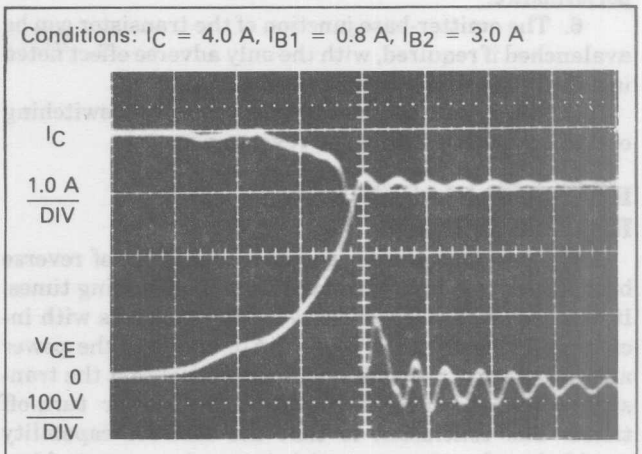


FIGURE 4(A), Voltage Source

$V_{BE(off)}$ = 3.0 V
t = 50 ns/DIV

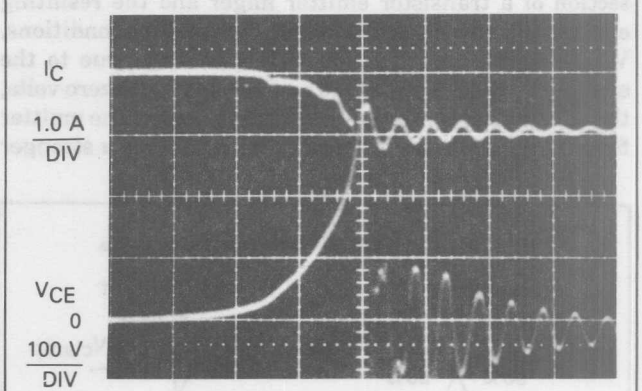


FIGURE 4(B), Current Source

$-V_2$ = 11 V

FIGURE 4, Inductive Turn-Off, 2N6547

TURN-OFF CONCLUSIONS

A study of these figures and the means of generating them lead to several interesting conclusions:

1. Storage time is the same for both a resistive load and an inductive load of the same peak collector current and the same I_{B2}, and decreases with increasing reverse bias.

2. Storage time is dependent on the magnitude of I_{B2} and independent of how it is derived, be it a voltage source or current source.

3. Fall-time is slightly faster for an inductive load than a resistive load. It decreases with increasing reverse bias to the point where I_{B2} approaches I_C and then starts to increase. This condition is attributed to the emitter having no further influence on the collector (I_E = 0) and the fall-time now measured is recovery time of the collector-base junction.

4. Crossover time decreases with increasing reverse bias resulting in lower inductive turn-off switching losses.

5. Reverse bias will greatly reduce turn-off times up to a point of diminishing returns. Further increase in $V_{BE(off)}$ or I_{B2} will not always result in better switching performance.

6. The emitter-base junction of the transistor can be avalanched if required, with the only adverse effect noted is a degradation of low current h_{FE}.

7. The circuit can be tailored to optimize switching operation by controlling the reverse bias.

REVERSE BIAS ENERGY RELATIONSHIPS

The previous section describes the effect of reverse bias on clamped inductive load turn-off switching times. It was shown that the crossover time decreases with increasing reverse bias (Figure 5(A)), and that the power and the energy (the area under the curve) that the transistor must dissipate are greater for slower turn-off times. The conclusion is that the RBSOA capability would therefore increase with increasing reverse bias. However, classical theory states that reverse biasing the transistor decreases the turn-off energy capability as illustrated in Figure 5(B). This figure shows the cross-section of a transistor emitter finger and the resulting emitter currents that flow under the two bias conditions, $V_{BE(off)}$ equals zero and 5.0 V respectively. Due to the small lateral field across the emitter-base with zero volts, the current flows relatively uniformly across the emitter finger; but when the larger off-bias is applied a stronger field results, causing the current to be concentrated at the center of the emitter. This pinching effect causes a greater current density, resulting in a hot spot with the device eventually going into second breakdown. This seeming contradiction in inductive turn-off energy capability will be addressed in the later section of this article describing the non-destruct RBSOA results.

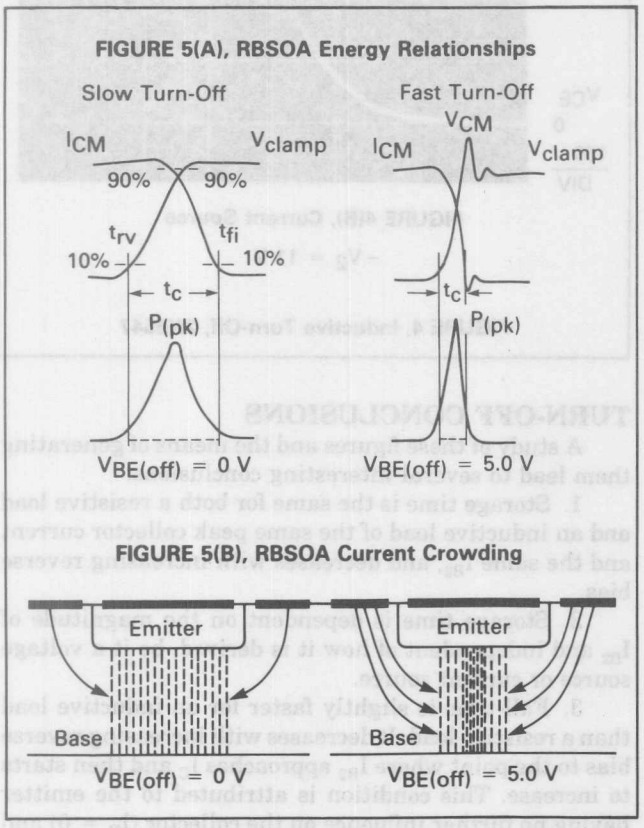


FIGURE 5(A), RBSOA Energy Relationships

FIGURE 5(B), RBSOA Current Crowding

FIGURE 5, The Effects of Current Crowding and Turn-Off Switching Speeds on RBSOA

DESTRUCT RBSOA TEST RESULTS

One of the first Switchmode Transistors* that was characterized for RBSOA, the 2N6545, was introduced in the mid-70's. Realizing that this device, during clamped inductive turn-off, had a different energy capability than the published forward bias SOA (FBSOA), a number of devices were then destructively tested to determine this energy limit. The results of this initial testing (Figure 6(A)) showed an energy capability to 450 V during turn-off which was described as $V_{CEX(SUS)}$; ($V_{CEO(SUS)}$ was specified as 400 V). Due to the limited data obtained at that time, the RBSOA curve published described a stepped rectangle, a condition that very seldom occurs in nature. Further experience in RBSOA characterization through destructive testing produced the two illustrated, but unpublished curves of $V_{BE(off)}$. Subsequently introduced Switchmode Transistors generally showed a full family of $V_{BE(off)}$ curves, as depicted by the RBSOA characterization of the plastic power transistors, MJE13006,7 of Figure 6(B). These curves were derived with a constant forced beta, usually five for discrete Switchmode Transistors. Note that the family of curves of $V_{BE(off)}$ shows an increasing RBSOA capability with reverse bias and that the maximum voltage limit is the specified V_{CEV} of 600 or 700 V. Also, at the high current end of the characterization all curves approach 300 V, a voltage below the specified $V_{CEO(SUS)}$ of 400 V, further illustrating the energy limits between RBSOA and FBSOA.

To generate the complete curves required destructive testing of as many as 100 devices, a costly and time consuming procedure. Usually five devices were tested at each selected collector current point; the clamp voltage was increased until the transistor failed. The resulting cluster of points would often be widespread, crossing over into other bias test points. This ambiguity somewhat complicates the drawing of the final derated RBSOA curves.

Figure 6(C) describes the RBSOA rating of the high voltage Switchmode Transistor MJ8508. This device has a V_{CEO} rating of 800 V and a V_{CEV} rating at low currents of 1400 V. As in all published Designer's Data Sheet curves, the transistors are characterized at an elevated junction or case temperature by bringing the heat sink on which the transistors are mounted to 100°C. The devices then are pulsed at low duty cycles to minimize the dissipative temperature rise.

NON-DESTRUCT RBSOA TEST RESULTS

In order to save the T.U.T. from the normally destructive second breakdown energy, the stored inductive energy must be quickly diverted from the transistor to an external crowbar circuit. A test fixture, based on the work done at the United States National Bureau of Standards[2], was designed to have the capability of crowbaring as much as 50 A and blocking or standing off 1000 V. The 10 A crowbarred propagation delay was about 70 ns

and the current rise time was about 40 ns. Triggering of the crowbar was accomplished by detecting the fast rate of change of the collapsing collector-emitter voltage once the device went into second breakdown. Using this test fixture, a complete RBSOA curve can often be formed using only one T.U.T., requiring as many as 30 or 40 crowbars (second breakdowns). Not all devices will survive so many crowbars without degradation or failure, but a large percentage do, allowing a relatively simple and non-ambiguous curve to be generated. Degradation is measured by a relatively large change in collector leakage current I_{CES} after testing; as an example, a change from 0.1 μA to about 5.0 μA. For this magnitude of leakage current change, subsequent retesting will usually show a decrease in device RBSOA capability.

FIGURE 6(A), First RBSOA Characterization Using the 2N6547

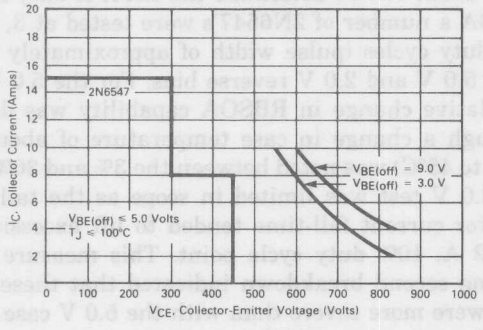


FIGURE 6(B), Typical RBSOA Characterization

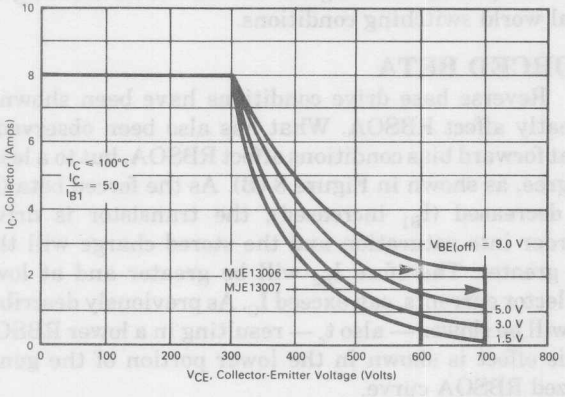


FIGURE 6(C), RBSOA Shown Out to V_{CEV} For High Voltage Transistor

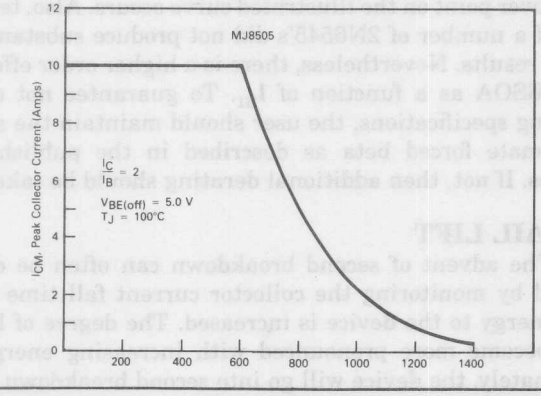


FIGURE 6,
RBSOA of High Voltage Power Switching Transistors

RBSOA VS. $V_{BE(off)}$

Figure 7(A) illustrates the actual characterization of a typical 2N6545 for RBSOA as a function of reverse bias $V_{BE(off)}$. For this 8.0 A device, there are two areas of interest. Note that the RBSOA capability of the device substantially increases with increasing reverse bias of from 1.5 V to 9.0 V at collector currents below about 6.0 A; at currents above this point, the opposite is true, but to a lesser degree. Recall that there are two factors affecting RBSOA capability versus reverse bias: turn-off switching speeds and current crowding. At currents below some nominal collector current, the switching speeds predominate and at values above, current crowding affects the performance. The crossover point is where the two effects balance each other. This crossover point, and the whole RBSOA curve for that matter, can vary from device to device even within the same product line. For other products, primarily some competitive lines using different processes, this crossover point occurred at a relatively low I_C indicating the predominance of current crowding.

To ensure that our devices meet the published data sheet curves, a number of devices from different wafer lots are tested and the results adequately derated for the final curves. Rather than show the relatively small deviation of curves at the high current end, we chose to simply draw the well derated curves approaching one point (Figure 6(B)). Also, for ease in characterizing the devices, we chose to generate the curves using $V_{BE(off)}$ as the variable. Using this technique, the forced beta is set for a particular I_C and $V_{BE(off)}$ can be readily varied for as many bias conditions as required. Recognizing that many applications use a current source for reverse biasing, we have lately also published the reverse input characteristic of the transistors, $V_{BE(off)}$ versus I_{B2}.

RBSOA VS. I_{B2}

The non-destruct test fixture also has the capability of generating the reverse base current I_{B2} using a current source. This is simply accomplished by adding an emitter resistor to the $V_{BE(off)}$ clamp transistor. To generate the RBSOA curves versus I_{B2} require somewhat more effort than the $V_{BE(off)}$ case as now, in addition to setting the forced beta, an I_{B2}/I_{B1} ratio must be set and maintained. The results of this exercise are shown in Figure 7(B) for a typical 2N6545. The family of reverse base current curves illustrated are for I_{B2} equal to I_{B1}, $2I_{B1}$ and $3I_{B1}$ respectively. As noted, RBSOA increases with increasing I_{B2} at low collector currents. Since two different devices were used in this exercise, each derived under two different conditions, an accurate comparison between the reverse biases can only be made when I_{B2} is normalized.

This comparison is illustrated in the photographs of Figures 4(A) and (B) where the peak I_{B2} was set equal for both the reverse voltage and constant current sources (3.0 A). I_{CM} was chosen to be 4.0 A, a point below the expected crossover point for the 2N6547 (15 A) transistor. Notice that the turn-off times, particularly t_c, are less for the current source. The point at which this transistor crowbarred for the voltage source was about 550 V whereas the current source configuration approached 900 V. However, when this device was retested at a higher collector current of 8.0 A with I_{B2} set to 5.0 A, both sources resulted in the same RBSOA point of about 420

FIGURE 7(A), Typical RBSOA for the 2N6545 as a Function of $V_{BE(off)}$

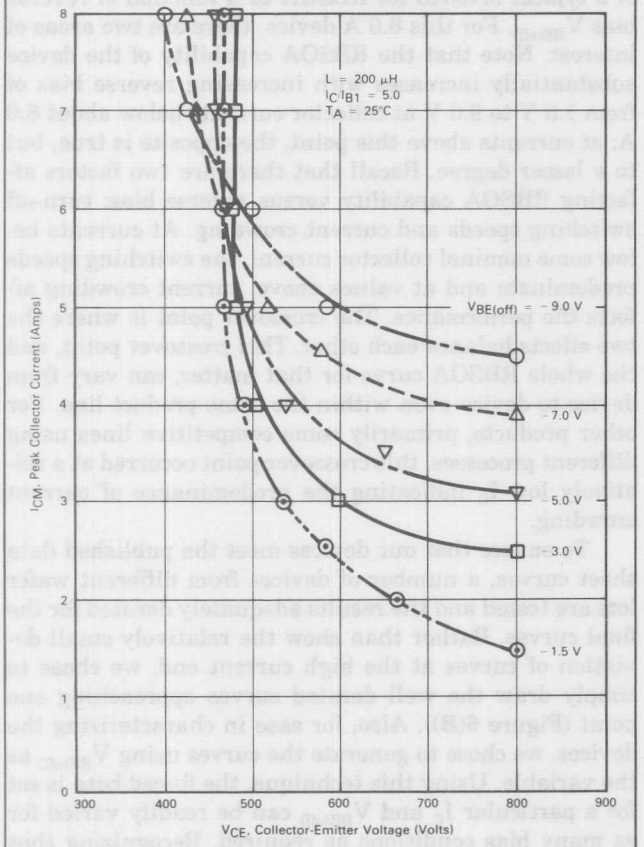
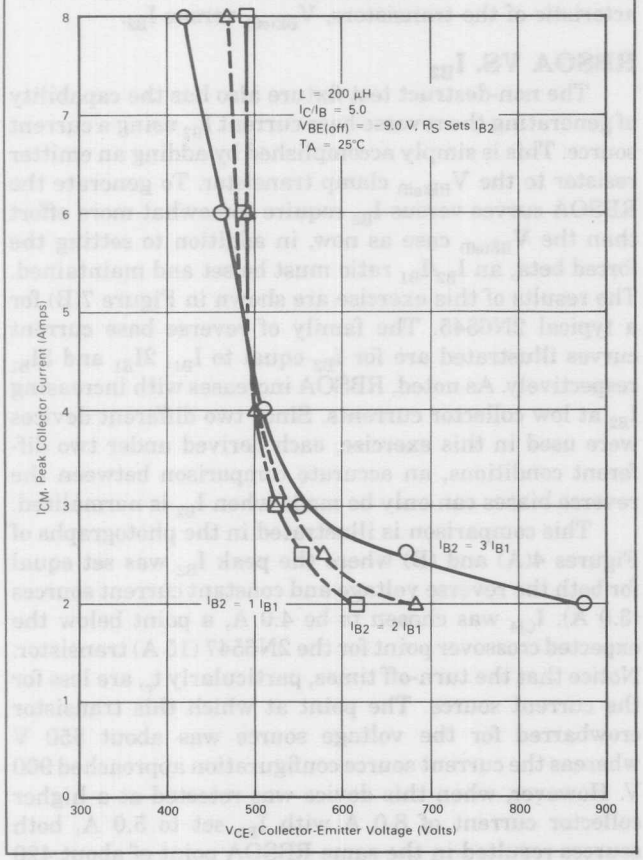


FIGURE 7(B), Typical RBSOA for the 2N6545 as a Function of I_{B2}



V even though the current source switched faster — current crowding evidently predominating. Using $V_{BE(off)}$ as the variable thus ensures a more conservative published curve.

TEMPERATURE

The effects of temperature on RBSOA for the 2N6547 are shown in Figure 8(A) for case temperatures of 25°C and 100°C. The 100°C temperature was derived by running the T.U.T. heat sink at the elevated temperature using power resistors as the heating element. As might be expected, the RBSOA capability was greater for the 25°C case temperature at the lower current portion of the curve. The small but opposite results at the higher current end were attributed to the increase in switching speeds at elevated temperature having a lesser effect on the current crowding phenomena.

All RBSOA tests were run at a low duty cycle, typically about 1%. To determine the effect of duty cycle on RBSOA a number of 2N6547's were tested at 3, 10 and 30% duty cycles (pulse width of approximately 80 μS) using 5.0 V and 2.0 V reverse bias. For the 5.0 V case, no relative change in RBSOA capability was detected although a change in case temperature of about 20°C (25°C to 45°C) was noted between the 3% and 30% cases. The 2.0 V test was limited in scope as the tail of the collector current fall-time tended to lift excessively at the 12 A, 10% duty cycle point. This measure of impending second breakdown indicated that these conditions were more severe than with the 5.0 V case.

Characterizing T.U.T.'s at 100°C case temperature and adequately derating the curves ensure meeting the real world switching conditions.

FORCED BETA

Reverse base drive conditions have been shown to greatly affect RBSOA. What has also been observed is that forward bias conditions affect RBSOA, but to a lesser degree, as shown in Figure 8 (B). As the forced beta (β_F) is decreased (I_{B1} increased), the transistor is driven harder into saturation and the stored charge will thus be greater. Therefore I_{B2} will be greater and at lower collector currents, can exceed I_C. As previously described, t_{fi} will be slower — also t_c — resulting in a lower RBSOA. This effect is shown in the lower portion of the generalized RBSOA curve.

Since this condition is dependent on I_{B2} and t_c, the results can be subjective and is reflected on where the crossover point on the illustrated curve occurs. Also, testing of a number of 2N6545's did not produce substantiative results. Nevertheless, there is a higher order effect on RBSOA as a function of I_{B1}. To guarantee not exceeding specifications, the user should maintain the approximate forced beta as described in the published curves. If not, then additional derating should be taken.

I_C TAIL LIFT

The advent of second breakdown can often be detected by monitoring the collector current fall time as the energy to the device is increased. The degree of lift can become more pronounced with increasing energy. Ultimately, the device will go into second breakdown as indicated by the crowbar firing. The change in V_{CL} to cause this effect can vary from a few volts to perhaps

several hundreds of volts with the larger change of voltage occurring at the low current — high voltage portion of the RBSOA curve — the low slope part of the curve where a small change in I_C can result in a large change in V_{CE}. Some extremely rugged products were able to sustain a full $E_{s/b}$ with the collector current lifting totally, and still devices did not go into second breakdown.

What constitutes an adverse degree of tail lift is quite subjective, be it 5% of I_{CM} at some point in time or 50%. It is presumed that the tail lift reflects the degree of hot spotting due to the increased turn off energy stresses. The long term effects of tail lift were determined by life testing ten (10) 2N6547's for about 1,000 hours with about a 20-30% tail lift — no adverse effects were noted.

To preclude the possible adverse effects of tail lift, the published RBSOA curve is based on either second breakdown or tail lift, whichever occurs first in terms of lower clamp voltage; thus a more conservative rating results.

FIGURE 8(A), The Effect of Case Temperature on RBSOA for a Typical 2N6547

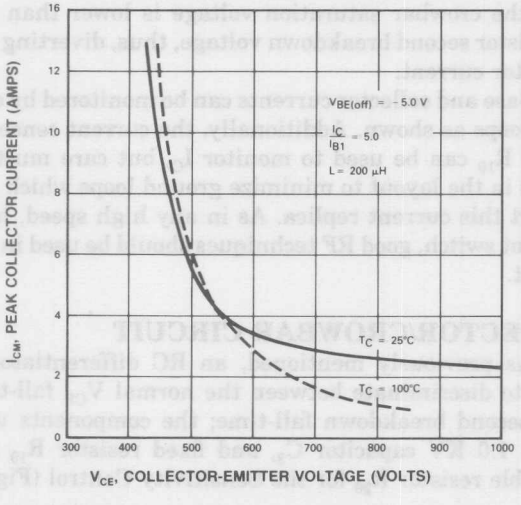
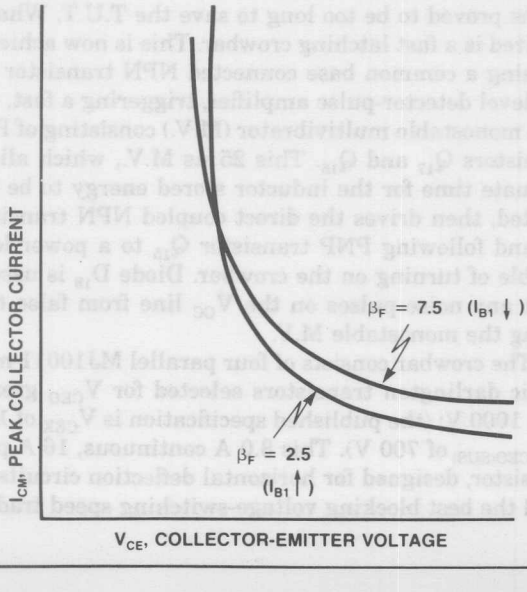


FIGURE 8(B), Typical RBSOA for the 2N6547 as a Function of Forced Beta β_F



NPN NON-DESTRUCT RBSOA TEST FIXTURE

The main elements of the NPN non-destruct RBSOA test fixture are illustrated in the block diagram of Figure 9(A). Of these blocks the most important ones are the Drive Circuit consisting of the I_{B1} and $V_{BE(off)}$ (or I_{B2}) Transistor Switches, the Detector/Crowbar and a Pulse Generator capable of being inhibited when crowbarring occurs. Of secondary importance are the V_{CC} Switch, the I_C Tail Sense circuit and a Greater Than 10% Duty Cycle Lockout circuit. Low current ± 12 V power supplies are also packaged into this system, but the required higher current, higher voltage supplies are not and must be externally connected to complete the system. To satisfy the 1000 V, 50 A capability of the non-destruct RBSOA system would require the following additional power supplies:

$+V_1$: 10 V @ 10 A pk (3.0 A cont)
$-V_2$: 10 V typ, 20 V max @ 15 A pk (3.0 A cont)
V_{CC}: 40 V max @ 50 A pk (10 A cont)
V_{CL}: 1000 V max @ 500 mA (a load resistor might be required to keep the supply in regulation).

Also required is an externally connected inductor, typically about 200 μH.

Referring to Figure 9A and also the RBSOA waveforms of Figure 9(B), circuit operation can be described as follows: An input pulse V_{IN} is applied to the input of the Drive Circuit controlling the three respective switches, I_{B1}, $V_{BE(off)}$ and V_{CC}. The I_{B1} Switch supplies postive base current and concurrent with its turnoff, the $V_{BE(off)}$ (I_{B2}) Switch is turned on. The resulting base voltage and current waveforms are as shown. The collector supply is also turned on (V_{CC} Switch) when positive base current is applied and will remain on for several microseconds (due to drive transistor storage time) after removal of the input pulse. During this on-time, the collector current ramps-up and upon turn off, the collector voltage flies back. When the flyback voltage reaches the clamp voltage, the inductor current is transferred to the clamp circuit. The collector voltage will then fall at a relatively slow rate, typically a couple of hundred nanoseconds, when the energy stored in the inductor is completely discharged.

If, however, excessive energy were applied to the T.U.T. during this switching time, the transistor could go into second breakdown, and then the collector voltage would fall very rapidly, possibly in less than 10 ns. When this occurs, the low R-C time constant Differentiator will detect this fast falling waveform — discriminating against the normal slow falling waveform — and produce a negative going pulse which ultimately triggers the Crowbar. The Crowbar fires and the current in the T.U.T. is quickly diverted to the Crowbar, removing the turnoff energy stress from the transistor. The Pulse Generator is also disabled, preventing any successive pulses from being reapplied until the system is reset.

Sometimes the collector current tail might lift prior to second breakdown (Figure 9(B)). In that case the I_C Tail Sense circuit can be used to automatically detect the degree of lift above a given reference level. This circuit consists of a variable delayed sample pulse to measure some point in time during the collector current fall-time, a sample and hold circuit to store the magnitude of this

current and a comparator with an adjustable threshold voltage. If the tail lift current exceeds the threshold, a latch SCR will fire, inhibiting the pulse generator.

DRIVE CIRCUIT

The Drive Circuit for the RBSOA test fixture is shown in Figure 10 and consists of the three aforementioned switches. A darlington transistor Q_1 is used to buffer the CMOS derived input pulse of +12 V from the Drive Circuit.

Forward base current I_{B1} is generated by turning on the NPN transistor Q_2 with the positive going input pulse. This stage, in turn, supplies drive to the PNP darlington configured constant current transistors Q_3 and Q_4, with the I_{B1} current being set by the course and fine control potentiometers R_2 and R_3 in the emitter circuit.

Reverse bias is derived by differentiating the input pulse with the R_1C_1 network. The generated negative going pulse, which is coincident with the trailing edge of the input pulse, then turns on PNP transistor Q_5 and the following discrete NPN darlington Q_6 and Q_7. In a similar manner to the I_{B1} Switch, I_{B2} is set by potentiometer R_5 and R_6. If the $V_{BE(off)}$ mode is required, the V-I switch S5, is thrown to short out the emitter resistors, thus applying $-V_2$ (less the saturation voltage of Q_6 and Q_7) to the base of the T.U.T. The off bias voltage pulse is set by R_1C_1 and for the values chosen is about 10 μs. Also, due to the trailing edge coincidence of the two pulses (plus approximately equal propagation delays through the two respective switches), the transition time between I_{B1} and I_{B2} can be relatively fast for some T.U.T.'s and operating conditions, approaching less than 200 ns.

With the component values and power supplies shown, I_{B1} and I_{B2} of 10 A and 15 A respectively can be reached when the input duty cycle is less than about 20%.

The Collector Switch is used as a safety factor, removing current from the inductor if the T.U.T. were to fail short. This circuit utilizes two cascaded Baker clamped monolithic darlingtons (NPN Q_8 and PNP Q_9) to reach the 50 A capability of the fixture. The Baker clamp diodes (D_2, D_3 and D_4, D_5) minimize the storage time of this switch after the T.U.T. is turned off.

Once the T.U.T. is turned off, the inductor stored energy is dissipated through the two clamp diodes (D_6 and D_7 for high voltage capability), the clamp supply and filter network, and Q_9 clamp diode D_{22}. Diodes D_8 and D_9 in the collector circuit of the T.U.T. are used to prevent reverse collector currents from flowing and also to ensure that the crowbar saturation voltage is lower than the transistor second breakdown voltage, thus, diverting the collector current.

Base and collector currents can be monitored by current loops as shown. Additionally, the current sense resistor R_{10} can be used to monitor I_C, but care must be taken in the layout to minimize ground loops which can distort this current replica. As in any high speed, high current switch, good RF techniques should be used in the layout.

FIGURE 9(A), Block Diagram of the NPN Non-Destruct RBSOA Test Fixture

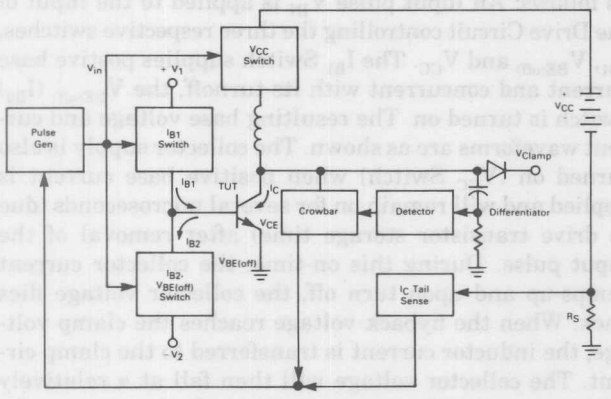
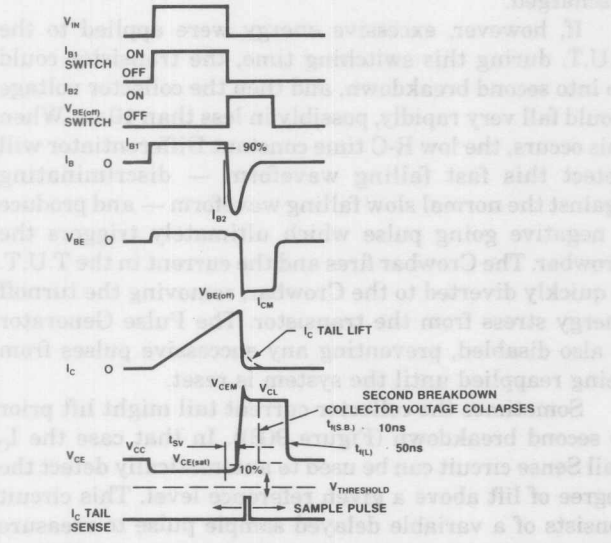


FIGURE 9(B), RBSOA Waveforms



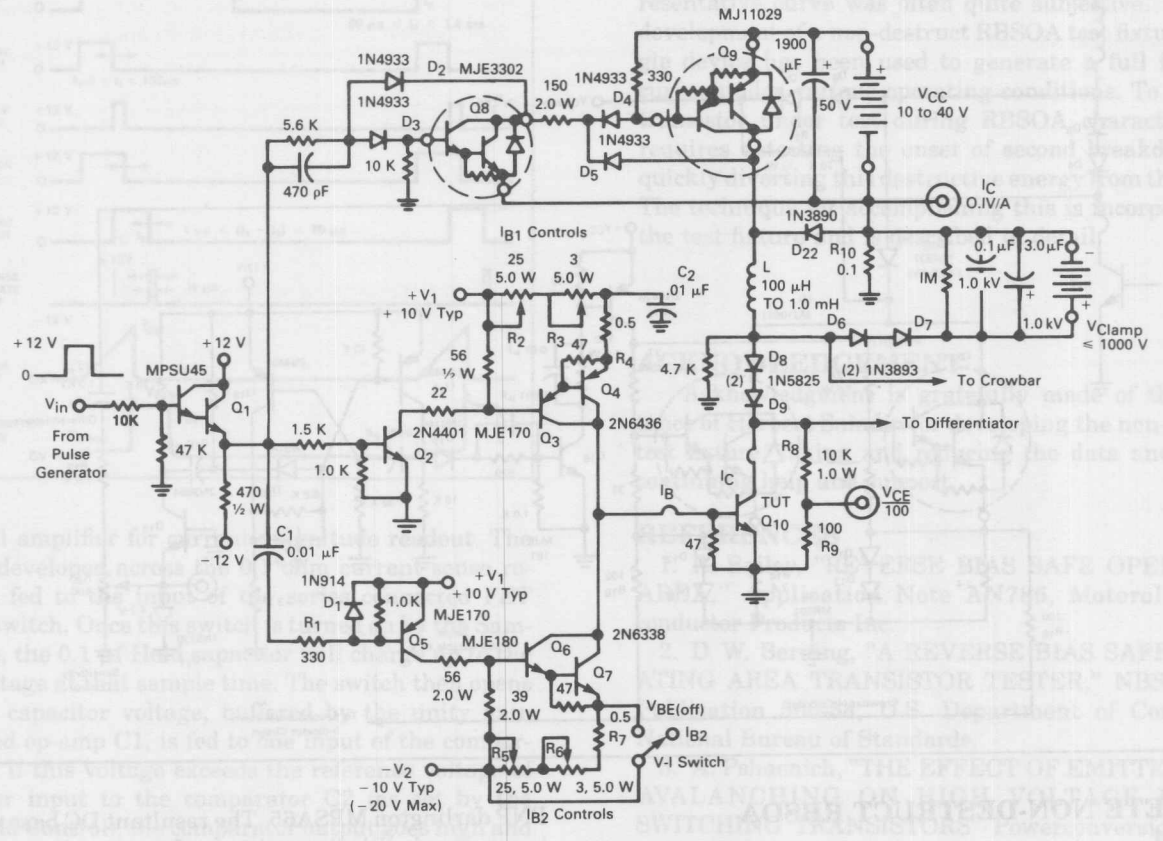
DETECTOR/CROWBAR CIRCUIT

As previously mentioned, an RC differentiator is used to discriminate between the normal V_{CE} fall-time and second breakdown fall-time; the components used are a 1.0 KV capacitor C_3, and fixed resistor R_{19} and variable resistor R_{20} for the Sensitivity Control (Figure 11).

Originally, the output pulse from this network fired a 25 A SCR as a crowbar, but the turn-on time of about 600 ns proved to be too long to save the T.U.T. What is required is a fast latching crowbar. This is now achieved by using a common base connected NPN transistor Q_{19} as a level detector-pulse amplifier, triggering a fast, discrete monostable multivibrator (M.V.) consisting of PNP transistors Q_{17} and Q_{18}. This 25 μs M.V., which allows adequate time for the inductor stored energy to be dissapated, then drives the direct coupled NPN transistor Q_{16} and following PNP transistor Q_{15} to a power level capable of turning on the crowbar. Diode D_{19} is used to block any noise pulses on the V_{CC} line from false triggering the monostable M.V.

The crowbar consists of four parallel MJ10011 monolithic darlington transistors selected for V_{CEO} greater than 1000 V; (the published specification is V_{CEX} of 1400 V, $V_{CEO(SUS)}$ of 700 V). This 8.0 A continuous, 16 A peak transistor, designed for horizontal deflection circuits, offered the best blocking voltage-switching speed tradeoff

FIGURE 10, Non-Destruct RBSOA Drive Circuit



of the several different devices tested. By using fast, wide band transistors throughout this Detector/Crowbar, propagation delay and rise time of 70 ns and 40 ns respectively were measured at I_C of 10 A.

Diode D_{10} and resistor R_{21} prevent possible high dv/dt flyback voltages from falsely turning on the crowbar.

The resistor-diode networks in the respective darlington emitter circuits serves both as a ballasting-voltage clipping circuit and a crowbar indication source for the second breakdown LED indicator circuit.

CONTROL CIRCUIT

The timing functions for the Non-Destruct RBSOA Test Fixture are generated in the Control Circuit (Figure 12(A)) which is derived primarily from two I.C.'s, the MC14001 Quad 2 Input NOR Gate and the MC14572 Hex Gate. These gates are configured into an astable M.V. and three monostable M.V.'s which produce the Pulse Generator output V_{IN} and the Sample Gate for the I_C Tail Sense sample and hold (S/H) circuit. Referring to Figure 12(A) and the timing waveforms of Figure 12(B), the astable M.V. (Gates A1 and A2) is the system clock which sets the repetition rate of V_{IN} (adjusted by the Rep Rate Control potentiometer for a period of from about 90 µs to 1.4 ms). The output of the clock then triggers the Pulse Width Monostable M.V. (when Switch S2 is in the Free Run position) consisting of NOR Gates A3 and A4. Pulse width variations of from about 4.0 µs to 180 µs are obtained with the Pulse Width Control potentiometer. This M.V. then triggers a fixed 5.0 µs M.V. (Gates B5 and B6) whose output is diode NOR'ed with the P.W.M.V. output. The result, after inversion by Gates B3 and B4, is that the V_{IN} pulse is thus variable in width by an additional 5.0 µs (9 µs to 185 µs). The reason for this pulse stretching technique is to allow the derived Sample Gate to be capable of "walking in" to at least the very peak of the collector current.

The leading edge of the 5.0 µs M.V. output then triggers the Sample Delay M.V. (Gates B1 and B2), variable from 1.0 to 70 µs with a potentiometer, whose output then drives the RC differentiating network in the base circuit of transistor Q_{20}. This normally on transistor, configured as half monostable M.V., will turn-off for the RC time constant, producing the approximately 0.5 µs wide Sample Gate. The Sample Gate, by virtue of the Delay Mono M.V., can thus be varied from a few µs proceeding the t_{fi} to about 70 µs thereafter.

The Control Circuit as described above will produce free running gates whose duty cycle should be maintained at less than 10% (limited by the Driver Circuit resistor power ratings). One-shot operation can also be generated by simply setting Switch S2 to the One Shot position and depressing the pushbutton Start Switch S3, thus providing a trigger to the Pulse Width Mono M.V.

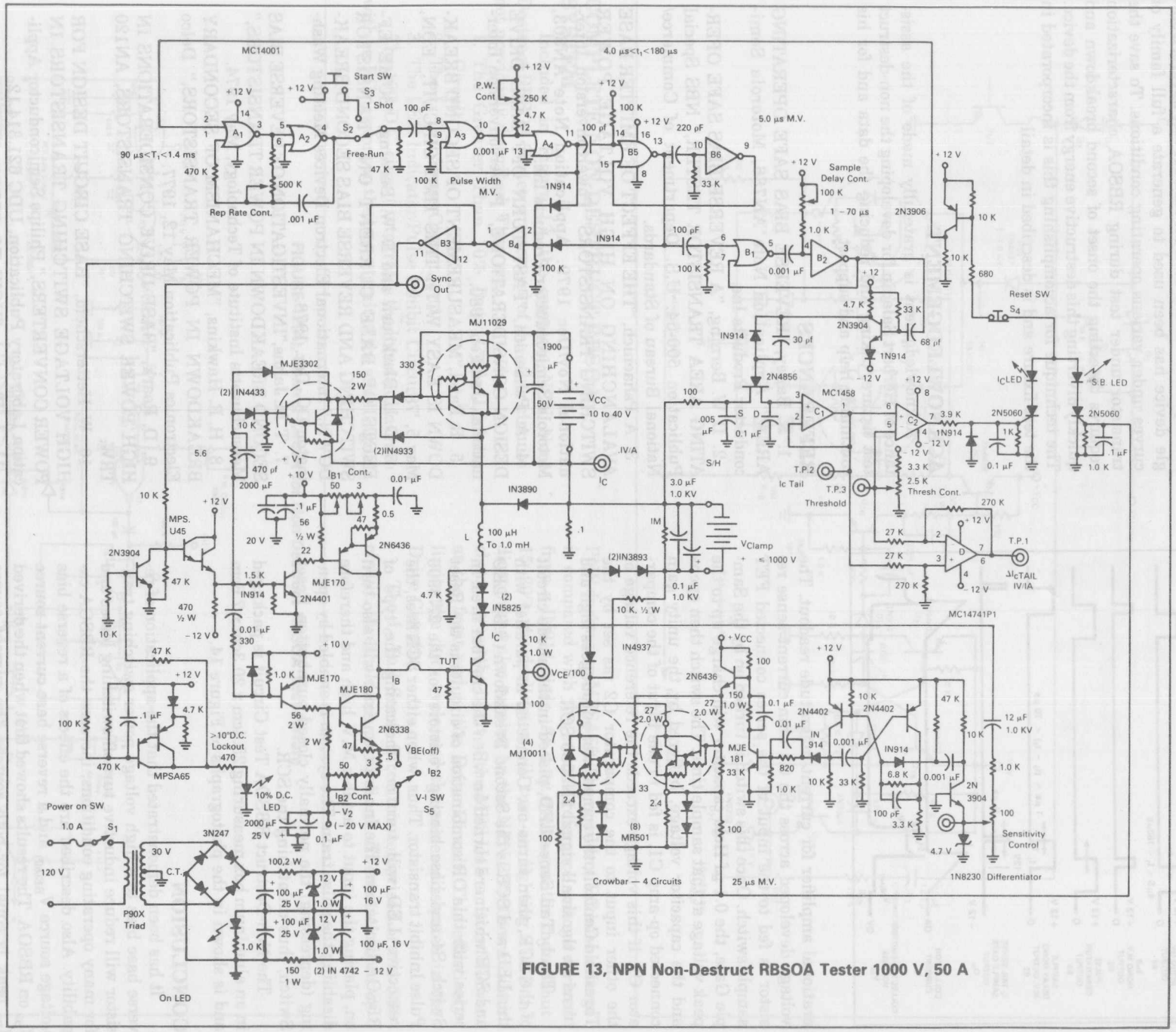


FIGURE 13, NPN Non-Destruct RBSOA Tester 1000 V, 50 A

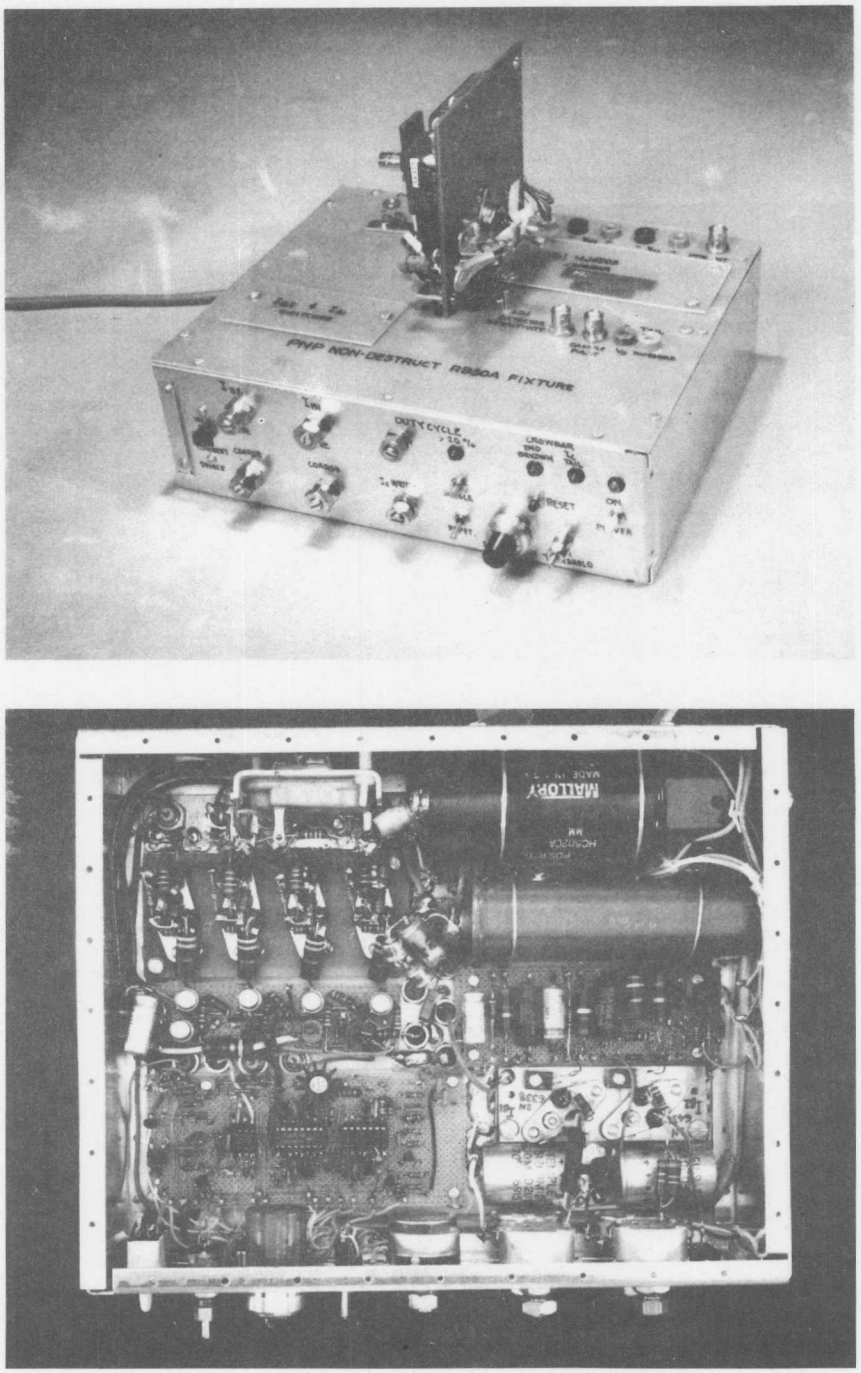


FIGURE 14, Non-Destruct RBSOA Fixture